IN THE CLAIMS:

Please amend the claims as follows:

1-63. (Canceled)

64. (Previously Presented) A computer system, comprising:

at least one processor; and

a memory;

wherein the computer system is configured to couple to an emulator, wherein the emulator is configured to emulate an integrated circuit designed to communicate bidirectionally with a computer peripheral device;

wherein the memory has computer instructions stored thereon that are executable by the at least one processor to cause the computer system to:

receive one or more digital data packets at a first transmission rate from the computer peripheral device;

store the digital data packets in a memory buffer;

retrieve the digital data packets from the memory buffer; and

send data contained in the received digital data packets to the emulator at a second transmission rate over a computer peripheral interface coupled to the computer system, wherein the second transmission rate is slower than the first transmission rate.

65. (Currently Amended) The computer system of claim 64, wherein the instructions are executable to cause the computer system to modify data in the received one or more digital data packets to a ~~make the~~ data format accepted by ~~suitable for transmission to~~ the emulator.

66. (Previously Presented) The computer system of claim 65, wherein the computer peripheral device is a network interface card; and

wherein the instructions are executable as a multi-threaded program.

67. (Previously Presented) The computer system of claim 64, wherein the emulator is incapable of receiving and processing data sent to the emulator at the first transmission rate.

68. (Previously Presented) The computer system of claim 65, wherein the emulator is implemented, at least in part, using field programmable gate arrays; and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to a design of the integrated circuit, wherein the design allows bidirectional communication with the computer peripheral device.

69. (Previously Presented) The system of claim 64, wherein the computer peripheral interface is a network connection; and

wherein the instructions are executable to cause the computer system to repackage data from the stored digital data packets.

70. (Previously Presented) The system of claim 65, wherein the instructions are executable to cause the computer system to log data corresponding to received data and/or sent data in a log file.

71. (Canceled)

72. (Previously Presented) The computer system of claim 65, wherein the received one or more digital data packets are variable in size.

73. (Previously Presented) A method, comprising:

a first computer receiving a plurality of data packets at a first transmission rate from a first computer peripheral device, wherein the computer includes at least one processor and a memory;

the first computer buffering one or more of the plurality of data packets in the memory, wherein the buffered one or more packets are destined for an emulator coupled to the first computer via an interface, wherein the emulator is configured to emulate a design of an integrated circuit used as a component of a second computer peripheral device, and wherein the integrated circuit is designed to communicate bidirectionally with the first computer peripheral device; and

the first computer sending data contained in the buffered one or more packets to the emulator via the interface at a second transmission rate that is slower than the first transmission rate.

74. (Previously Presented) The method of claim 73, wherein the data sent to the emulator is usable to debug the design of the integrated circuit; and

wherein the interface is a network connection.

75. (Previously Presented) The method of claim 73, further comprising:

the first computer repackaging data from the buffered data packets;

wherein the repackaged data is the data sent from the first computer to the emulator.

76. (Previously Presented) The method of claim 73, further comprising:

the emulator receiving and processing the data sent by the first computer, wherein said processing is performed, at least in part, according to the design of the integrated circuit.

77. (Previously Presented) The method of claim 76, further comprising the emulator sending data corresponding to the received and processed data to a second computer.

78. (Previously Presented) The method of claim 73, wherein the emulator is configured to emulate a network interface card, wherein the integrated circuit is designed to be a component of the network interface card; and

wherein the first transmission rate is a data rate of an ethernet network.

79. (Previously Presented) The method of claim 73, further comprising the first computer, for each data packet received:

examining that data packet;

determining if that data packet is addressed to the emulator, wherein the emulator is configured to emulate a network interface card; and

if that data packet is addressed to the emulator, buffering that data packet and sending data contained in the buffered packet to the emulator at the second transmission rate.

80. (Previously Presented) The method of claim 73, wherein the emulator is implemented, at least in part, using field programmable gate arrays; and

wherein the field programmable gate arrays are operable to be programmed with a hardware model corresponding to the design of the integrated circuit.

81. (Currently Amended) A ~~non-transitory~~ computer-readable storage medium having instructions stored thereon that are executable by at least one processor to cause a computer system including the at least one processor to perform operations that include:

receiving, at a first transmission rate, one or more digital data packets sent from a computer peripheral device;

buffering the received digital data packets within a memory of the computer system; and

at a second transmission rate that is slower than the first transmission rate, sending data contained in the buffered digital data packets to an emulator that is coupled to the computer system via a computer peripheral interface, wherein the emulator is configured to receive and process the sent data according to a design of an integrated circuit being emulated, wherein the integrated circuit is designed to communicate bidirectionally with the computer peripheral device.

82. (Previously Presented) The non-transitory computer-readable medium of claim 81, wherein the operations further include, for each digital data packet received by the computer system:

examining that digital data packet;

determining if that digital data packet is addressed to the emulator; and

buffering that digital data packet and sending data contained in that buffered packet to the emulator only if that digital data packet is addressed to the emulator.

83. (Previously Presented) The non-transitory computer-readable medium of claim 81, wherein the computer peripheral device is a network device and wherein the received one or more digital data packets are transmitted from the network device via a network connection according to a network communications protocol.

84. (Previously Presented) The non-transitory computer-readable medium of claim 81, wherein the operations further include repackaging the data contained in the buffered data packets prior to sending the data to the emulator at the second transmission rate.

85. (Previously Presented) The non-transitory computer-readable medium of claim 81, wherein the emulator is configured to receive and process data sent at the second transmission rate, but is not configured to receive and process data sent at the first transmission rate.

86. (Previously Presented) The non-transitory computer-readable medium of claim 81, wherein the computer peripheral device is coupled to a different computer system, wherein the different computer system is configured to send data from the computer peripheral device via a network interface, and wherein the network interface is the computer peripheral interface.

87. (Currently Amended) A method comprising:

receiving digital data from a circuit emulator at a program running on at least one processor of a computer, wherein the digital data is received at a first transmission rate, and wherein the circuit emulator is configured to emulate an integrated circuit that is designed to communicate bidirectionally with a computer peripheral device;

~~the program~~ storing the received data in a memory of the computer, wherein said storing is performed by the program;

~~the program~~ retrieving the stored data from the memory, wherein said retrieving is performed by the program; and

~~the program~~ transmitting the retrieved data to the computer peripheral device at a second transmission rate over a computer peripheral interface coupled to the computer, wherein the first transmission rate is slower than the second transmission rate, and wherein said transmitting is performed by the program.

88. (Previously Presented) The method of claim 87, wherein the circuit emulator is incapable of receiving and processing data transmitted to the circuit emulator at the second transmission rate.

89. (Currently Amended) The method of claim 87, further comprising ~~the program~~ keeping a record of the data received from the circuit emulator, wherein the received data is usable to optimize and/or debug a design of the integrated circuit.

90. (Currently Amended) The method of claim 87 further comprising ~~the program~~ modifying the received data from the circuit emulator to a ~~make the~~ data format accepted by ~~suitable for transmission to~~ the computer peripheral device, wherein said modifying is performed by the program.

91. (Previously Presented) The method of claim 87, wherein said receiving data from the circuit emulator is executed in a first thread, and said transmitting the data received from the circuit emulator is executed in a second thread; and

wherein the computer peripheral device is a network interface device.

92. (Previously Presented) A computer system, comprising:

at least one processor; and

a memory having computer instructions stored thereon that are executable by the at least one processor to cause the computer system to perform operations including:

receiving digital data from a circuit emulator at a first transmission rate, wherein the circuit emulator is configured to emulate an integrated circuit that is designed to communicate bidirectionally with a computer peripheral device;

storing the received data within the computer system;

retrieving the stored data from within the computer system; and

transmitting the retrieved data to the computer peripheral device at a second transmission rate over a computer peripheral interface coupled to the computer system, wherein the first transmission rate is slower than the second transmission rate.

93. (Previously Presented) The computer system of claim 92, wherein the circuit emulator is incapable of receiving and processing data transmitted to the circuit emulator at the second transmission rate.

94. (Currently Amended) The computer system of claim 92, wherein the operations further include modifying the received data from the circuit emulator to a ~~make the~~ data format accepted by ~~suitable for transmission to~~ the computer peripheral device.

95. (Previously Presented) The computer system of claim 92, wherein the operations further include keeping a record of the data transmitted to the computer peripheral device.

96. (Previously Presented) The computer system of claim 92, wherein the operations further include recording the throughput of the transmitted data.

97. (Previously Presented) A non-transitory computer-readable medium having stored thereon computer instructions that are executable by a computing device to cause the computing device to perform operations including:

receiving digital data from a circuit emulator at a first transmission rate, wherein the circuit emulator is configured to emulate an integrated circuit that is designed to communicate bidirectionally with a computer peripheral device;

storing the received data in a memory of the computing device;

retrieving the stored data from the memory; and

transmitting the retrieved data at a second transmission rate to the computer peripheral device over a computer peripheral interface coupled to the computing device, wherein the first transmission rate is slower than the second transmission rate.

98. (Previously Presented) The non-transitory computer-readable medium of claim 97, wherein the second transmission rate exceeds a transmission rate at which the circuit emulator is capable of receiving and processing data transmitted to the circuit emulator.

99. (Currently Amended) The non-transitory computer-readable medium of claim 97, wherein the operations further include modifying the received data to a ~~make the~~ data format accepted by ~~suitable for transmission to~~ the computer peripheral device.

100. (Previously Presented) The non-transitory computer-readable medium of claim 97, wherein the operations further include keeping a record of the data received from the circuit emulator and the data transmitted to the computer peripheral device, wherein the received data and the transmitted data are usable to optimize and/or debug a design of the integrated circuit.

101. (Previously Presented) The non-transitory computer-readable medium of claim 97, wherein said receiving digital the data operations further include recording the throughput of the transmitted data.